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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,011	12/13/2001	Laurent A. Six	TI-29536	2461

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,011	SIX, LAURENT A.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4-9, 11-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 4-9, 11-18 and 20 have been examined. The amendment dated 09/13/2004 has been entered.

Claim Rejections - 35 USC § 112

2. The rejection claims 3, 4, 10, 11, 19 and 20 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement on page 2, ¶ 2 of the Office Action dated 05/07/2004 has been overcome by the Applicant by canceling claims 3, 10 and 19. The Examiner withdraws the rejection.

Response to Arguments

Applicant's arguments filed 09/13/2004 have been fully considered but they are not persuasive. For ease of readability the rejection of claims 3, 10 and 19 on page 7, ¶ 4 have been incorporated into the rejection for claims 1, 9 and 16 on page 3, ¶ 3 of the Office Action dated 05/07/2004. No new grounds of rejection have been introduced.

The Applicant states "The features recited in this language so incorporated is neither taught nor suggested by either Kurtulik et al. or by Rearick", and also, "Rearick does not cure the deficiencies of Kudulik". The Examiner disagrees because Rearick suggests the state of the TAP controller 130 is controlled by a test clock and a test mode select signal (switch mode). Rearick discloses that during normal operation of the host (functional mode), the TAP is forced into the Test-Logic-Reset state by driving the

test mode select signal high and applying six or more test clock pulses. In this state, Rearick explains, the TAP issues a reset signal that places all test logic in a condition that does not impeded normal operation of the host (receives functional data over a test line while in switch mode). (Col. 8, lines 1-16).

The Applicant states "Rearick apparently relates to a method for reducing stored patterns for IC test by embedding BIST circuitry for chip logic into a scan test access port. It therefore has a different purpose than that of the claimed invention, namely, that of providing context save and restore using a scan chain". In response to applicant's argument above, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

In response to applicant's arguments, the recitation "providing context save and restore using a scan chain" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re*

Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the scan paths are used, qua scan paths, to scan normal data, as is recited in the claims) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is the Examiner's conclusion that claims 1, 9 and 16 as amended are not patentably distinct or non-obvious over the prior art of record namely, Kurtulik et al. (US2002/0125907) in view of Rearick (US 6715105). Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, 4-9, 11-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurtulik et al. (US2002/0125907), hereinafter Kurtulik, in view of Rearick (US 6715105), hereinafter Rearick.

Claims 1, 9, and 16:

Kurtulik teaches in Fig. 6 the ABIST engine 602 (state machine) generates word addresses, bit addresses, data-in, clocks and controls 604, as a serial stream of bits and shifts the data to the appropriate arrays 612 (device memory) via the scan chain 610. (Page 4, ¶ 41).

"a state machine operable to divide the scan chain into a plurality of sub-chains,"

Kurtulik teaches the scan chain 610 is reconfigured during scan ABIST mode to a shorter array sub-chain. (Page 4, ¶ 41).

"to provide a first data set in the sub-chains,"

Kurtulik teaches ABIST engine 602 (state machine) generates data-in as a serial stream of bits and shifts the data to the appropriate arrays 612 (device memory) via the scan chain 610. (Page 4, ¶ 41).

"to link the sub-chains in parallel,"

Kurtulik teaches the scan chain 704 is configured as a number of parallel sub-chains. (Page 4, ¶ 43).

"to link the sub-chains to the device memory,"

Kurtulik teaches the ABIST engine 602 (state machine) generates word addresses, bit addresses, data-in, clocks and controls 604, as a serial stream of bits and shifts the data to the appropriate arrays 612 (device memory) via the scan chain 610. Kurtulik also teaches the ABIST engine 602 (state machine) writes and reads data from the array 612 (linking sub-chains to the write port and read port of the memory device, from claim 9). (Page 4, ¶ 41).

"to execute a first application to update the first data set in the sub-chains, the first application operable to use the channel,"

Kurtulik teaches various algorithms programmed into the ABIST engine can supply different data-in patterns and address stepping to the array 612. (Page 4, ¶ 41).

"to shift the updated first data set into the device memory for storage,"

Kurtulik teaches a single operation performed on all arrays, for example a write, requires that the entire sub-chain be scanned with the address and data-in patterns for each array 612. (Page 4, ¶ 41).

"to shift a second data set from the device memory into the sub-chains, and to execute a second application to update the second data set in the sub-chains, the second application operable to use the channel."

Kurtulik teaches the controls and write clock 604 are activated once the scan in 606 address and data are set up, and all arrays 612 are written simultaneously. Kurtulik further teaches that the entire sub-chain is then reloaded serially (second data set) by the ABIST engine 602 to set up for the next array operation. (Page 4, ¶ 41).

Kurtulik does not explicitly teach "a switch mode for switching between applications", however, Kurtulik does teach the ABIST engine 602 (state machine) generates word addresses, bit addresses, data-in, clocks (test and functional) and controls 604, as a serial stream of bits and the scan chain 610 is reconfigured during scan ABIST mode (test mode). (Page 4, ¶ 41). Rearick teaches data (test data) is scanned into one or more scanpaths 172 from a scan data in (SDI) port 122 (test line) under the control of a scan clock signal SCAN_CLK 126 (test clock), either directly or

indirectly through a linear feedback shift register (LFSR) 102. Rearick further teaches the system execution clock CLK 109 (functional clock) is used to capture normal system data (functional data) into the registers comprising the scan path. (Col. 5, lines 60-67; col. 6, lines 1-6). Rearick also suggests the state of the TAP controller 130 is controlled by a test clock and a test mode select signal (switch mode). Rearick discloses that during normal operation of the host (functional mode), the TAP is forced into the Test-Logic-Reset state by driving the test mode select signal high and applying six or more test clock pulses. In this state, Rearick explains, the TAP issues a reset signal that places all test logic in a condition that does not impeded normal operation of the host (receives functional data over a test line while in switch mode). (Col. 8, lines 1-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurtulik's ABIST engine 602 (state machine) with Rearick's TAP controller 130 (also a state machine) to include Rearick's test mode select signal (switch mode) in the generatation of Kurtulik's clocks (test and functional) and controls 604. The artisan would be motivated to do so because this would enable Kurtulik's ABIST engine 602 to switch modes of applications between test and functional mode in loading data into the memory array 612.

Claim 2:

Kurtulik teaches a write operation performed on all arrays requires that the entire sub-chain be scanned with the address and data-in patterns for each array 612 (shifting through the writer port). Kurtulik teaches the data-out register from each array 612 (read port) feeds a dedicated MISR 618 forming an accumulated signature representing the

compressed output data from that array 612. The MISR 618 for each array 612 (device memory) are in the ABIST sub-chain. (Page 4, ¶ 41 and 42).

Claims 4, 11 and 20:

These claims are rejected per claims 1, 9, and 16. Kurtulik teaches various algorithms programmed into the ABIST engine (state machine) can supply different data-in patterns and address stepping to the array 612 (storing/shifting third and fourth data set). Kurtulik also teaches the ABIST engine 602 reloads the array for the next operation (restoring/shifting third and fourth data set). (Page 4, ¶ 41 and 42).

Claims 5 and 12:

These claims are rejected per claims 1, 9, and 16. Kurtulik teaches various algorithms programmed into the ABIST engine (state machine) can supply different data-in patterns and address stepping to the array 612 (storing/shifting third and fourth data set). Kurtulik also teaches the ABIST engine 602 reloads the array for the next operation (restoring/shifting third and fourth data set). (Page 4, ¶ 41 and 42).

Claims 6 and 13:

Kurtulik teaches the present invention is a method for testing semiconductor integrated circuits (ASIC, FPGA). (Page 1, ¶ 2 and 12).

Claims 7, 14 and 17:

Kurtulik teaches the ABIST engine 602 generates word addresses, bit addresses, data-in, clocks and controls 604, as a serial stream of bits and shifts the data to the appropriate arrays via the scan chain. Scan chains inherently include flip-flops as the clocked sequential elements in the chain or sub-chains. (Page 4, ¶ 41).

Claims 8, 15 and 18:

Kurtulik teaches the ABIST engine 602 (state machine) generates word addresses, bit addresses, data-in, clocks and controls 604, as a serial stream of bits and shifts the data to the appropriate arrays 612 (device memory) via the scan chain 610. Kurtulik further teaches the scan chain 610 is reconfigured during scan ABIST mode to a shorter array sub-chain with only the necessary data and address bits (specified number of sub-chains correspond to the data width of the device memory) to be scanned in 606 for each array sub-chain. (Page 4, ¶ 41).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

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